FIG. 1

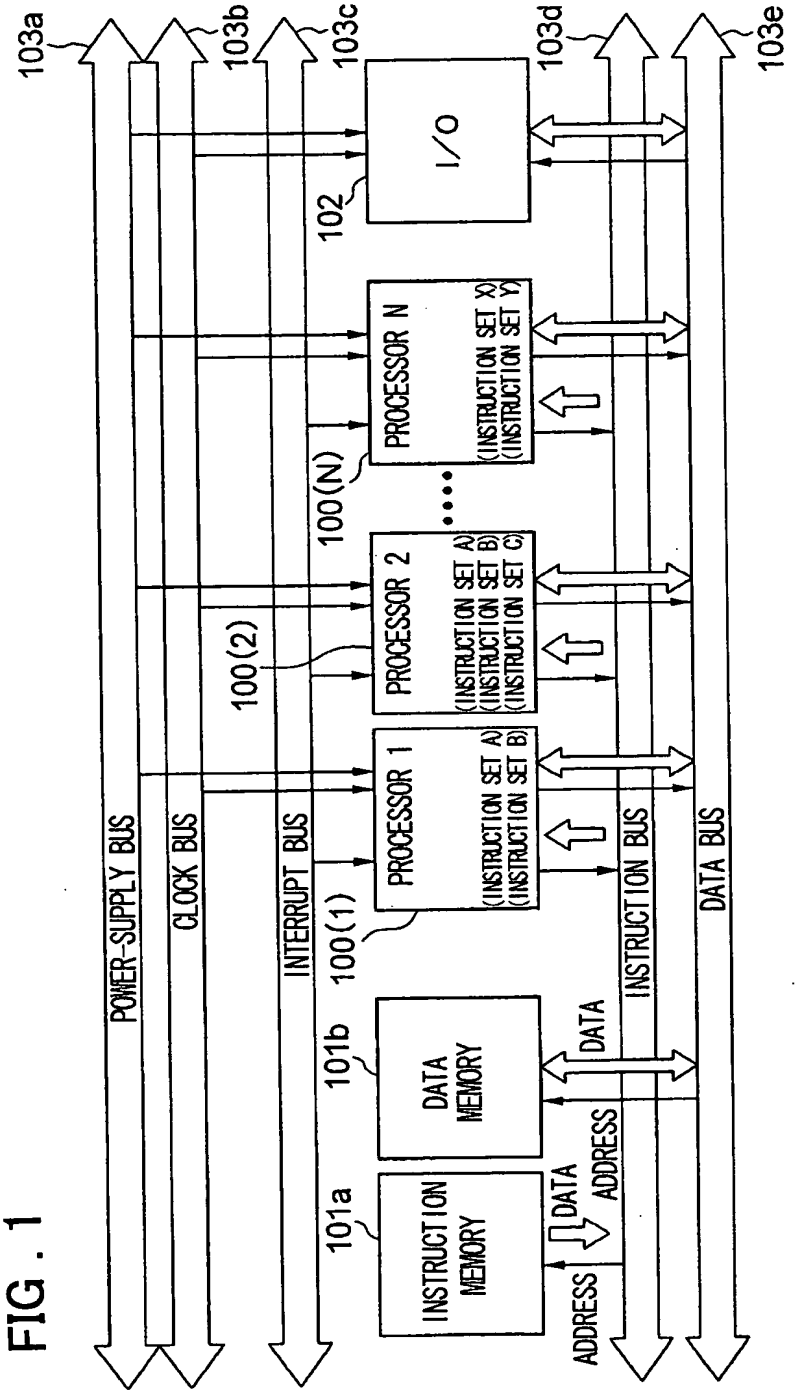

103a
103b
103c
103d
103e
POWER-SUPPLY BUS
CLOCK BUS
INTERRUPT BUS
INSTRUCTION BUS
DATA BUS
I/O
102
PROCESSOR N
(INSTRUCTION SET X)
(INSTRUCTION SET Y)
100(N)
PROCESSOR 2
(INSTRUCTION SET A)
(INSTRUCTION SET B)
(INSTRUCTION SET C)
100(2)
PROCESSOR 1
(INSTRUCTION SET A)
(INSTRUCTION SET B)
100(1)
DATA MEMORY
101b
INSTRUCTION MEMORY
101a
DATA
ADDRESS
DATA
ADDRESS

FIG. 2

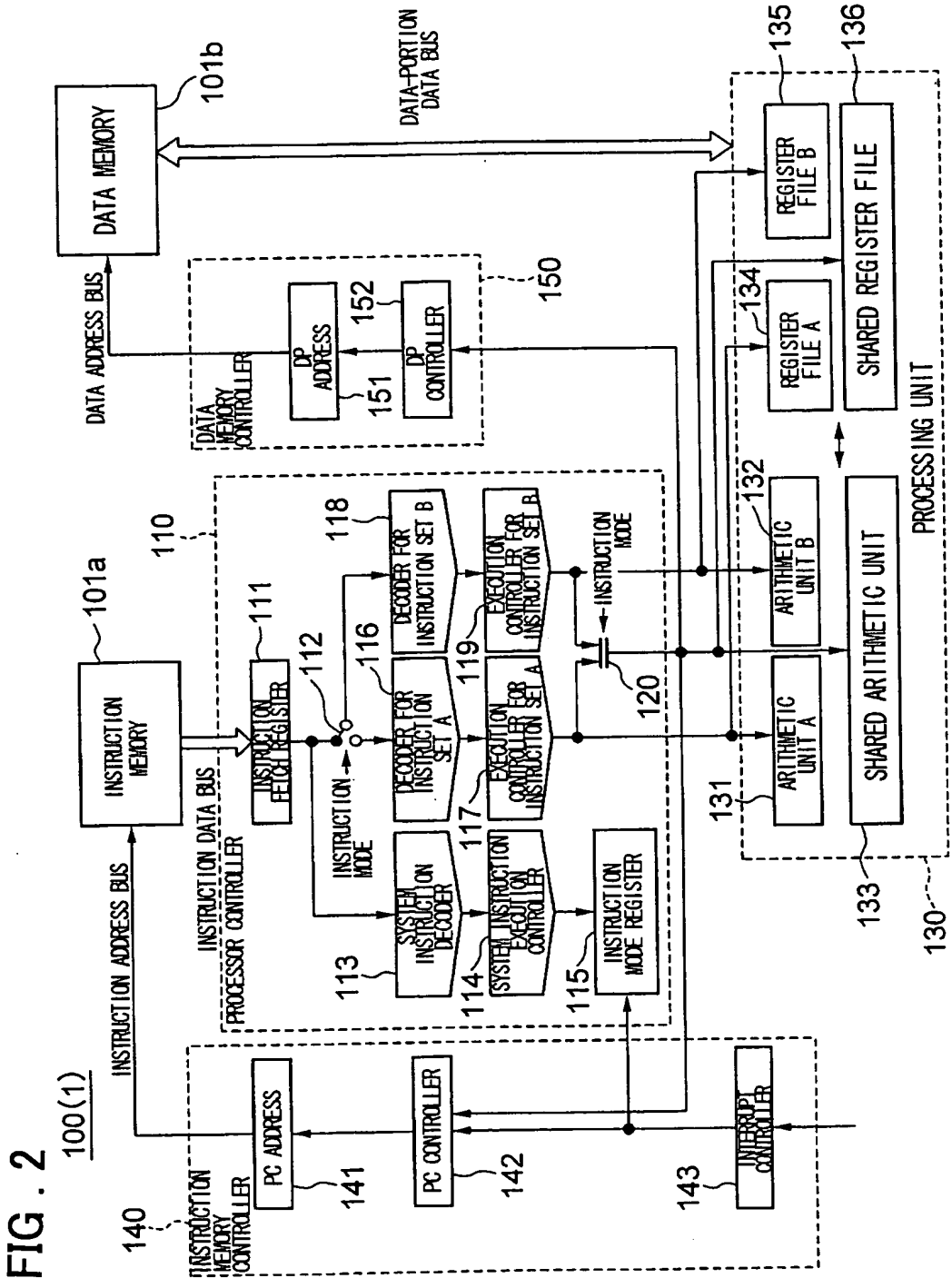
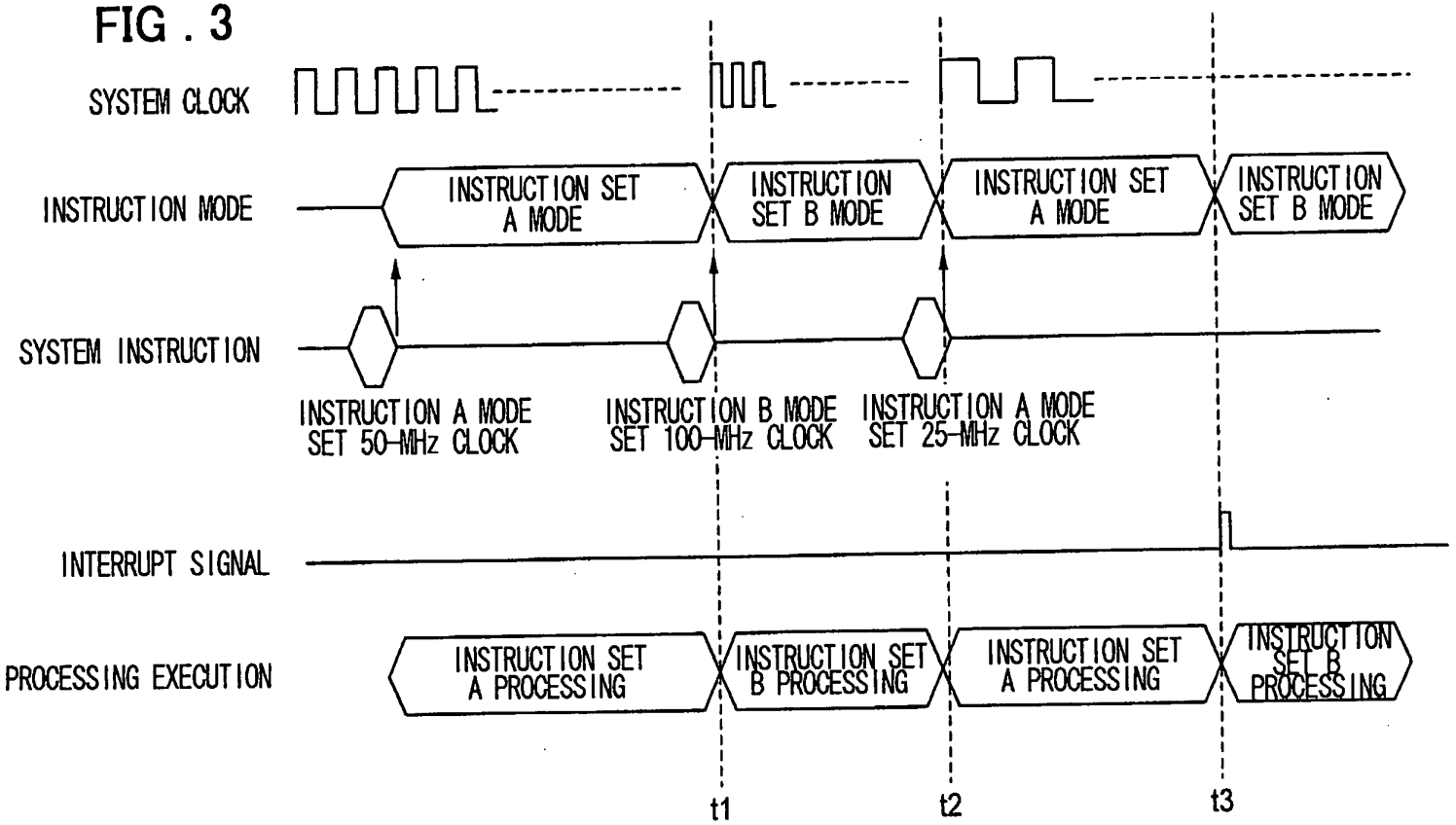

100(1)
DATA MEMORY
101b
DATA-PORTION DATA BUS
DATA ADDRESS BUS
DATA MEMORY CONTROLLER
DP ADDRESS
DP CONTROLLER
150
151
152
INSTRUCTION MEMORY
101a
INSTRUCTION ADDRESS BUS
INSTRUCTION DATA BUS
PROCESSOR CONTROLLER
110
INSTRUCTION FETCH REGISTER
111
112
INSTRUCTION MODE
DECODER FOR INSTRUCTION SET A
116
DECODER FOR INSTRUCTION SET B
118
EXECUTION CONTROLLER FOR INSTRUCTION SET A
117
EXECUTION CONTROLLER FOR INSTRUCTION SET B
119
INSTRUCTION MODE
120
SYSTEM INSTRUCTION DECODER
113
SYSTEM INSTRUCTION EXECUTION CONTROLLER
114
INSTRUCTION MODE REGISTER
115
INSTRUCTION MEMORY CONTROLLER
140
PC ADDRESS
141
PC CONTROLLER
142
INTERRUPT CONTROLLER
143
REGISTER FILE B
135
REGISTER FILE A
134
SHARED REGISTER FILE
136
ARITHMETIC UNIT B
132
ARITHMETIC UNIT A
131
SHARED ARITHMETIC UNIT
133
PROCESSING UNIT
130

FIG . 3



INSTRUCTION SET A: CONTROL-PERFORMANCE ORIENTED (CPU)
INSTRUCTION SET B: SIGNAL-PROCESSING-PERFORMANCEORIENTED (DSP)

FIG. 4

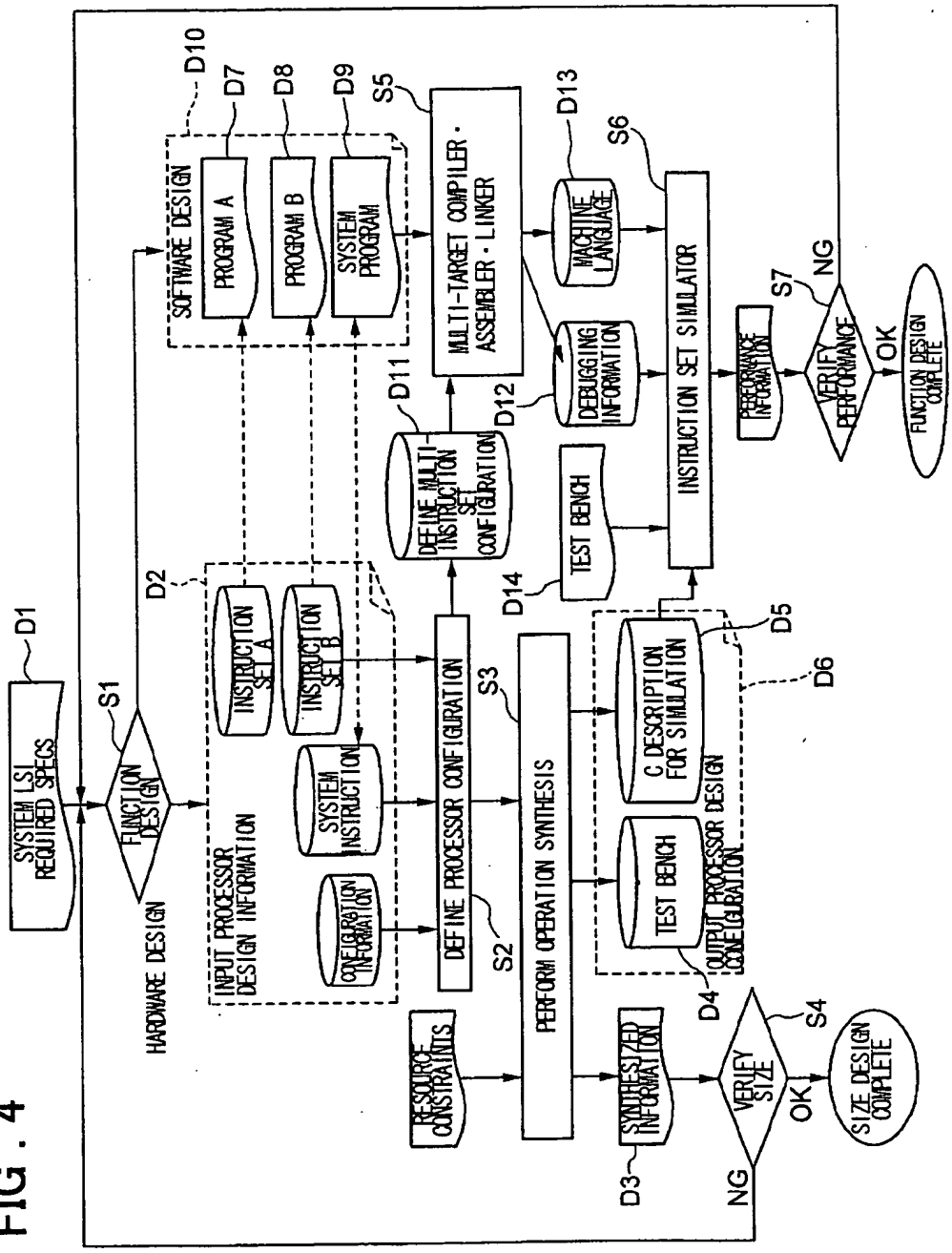

SYSTEM LSI REQUIRED SPECS
D1
FUNCTION DESIGN
S1
HARDWARE DESIGN
SOFTWARE DESIGN
D10
PROGRAM A
D7
PROGRAM B
D8
SYSTEM PROGRAM
D9
S5
MULTI-TARGET COMPILER · ASSEMBLER · LINKER
D13
MACHINE LANGUAGE
S6
DEBUGGING INFORMATION
D12
PERFORMANCE INFORMATION
S7
NG
VERIFY PERFORMANCE
OK
FUNCTION DESIGN COMPLETE
INSTRUCTION SET SIMULATOR
TEST BENCH
D14
D2
INPUT PROCESSOR DESIGN INFORMATION
INSTRUCTION SET A
INSTRUCTION SET B
SYSTEM INSTRUCTION
CONFIGURATION INFORMATION
DEFINE MULTI-INSTRUCTION SET CONFIGURATION
D11
DEFINE PROCESSOR CONFIGURATION
S2
S3
PERFORM OPERATION SYNTHESIS
RESOURCE CONSTRAINTS
C DESCRIPTION FOR SIMULATION
D5
D6
TEST BENCH
OUTPUT PROCESSOR CONFIGURATION
D4
SYNTHESIZED INFORMATION
D3
VERIFY SIZE
S4
NG
OK
SIZE DESIGN COMPLETE
HARDWARE DESIGN

FIG . 5a

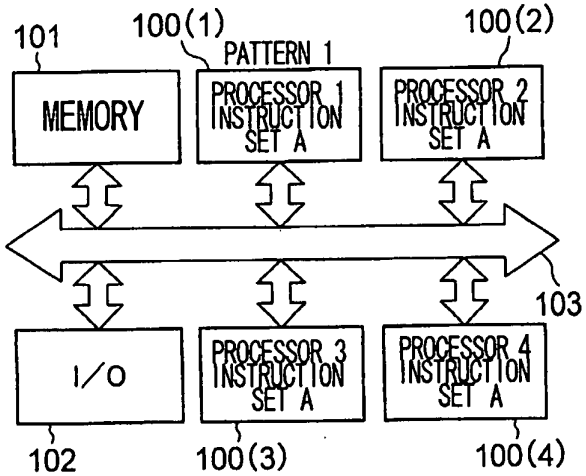


FIG . 5b

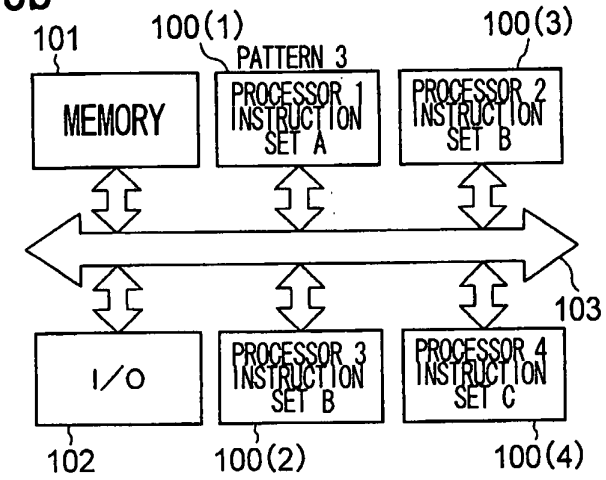


FIG . 5c

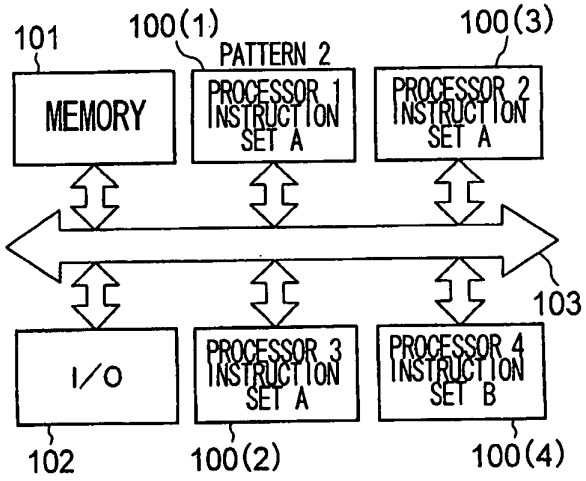
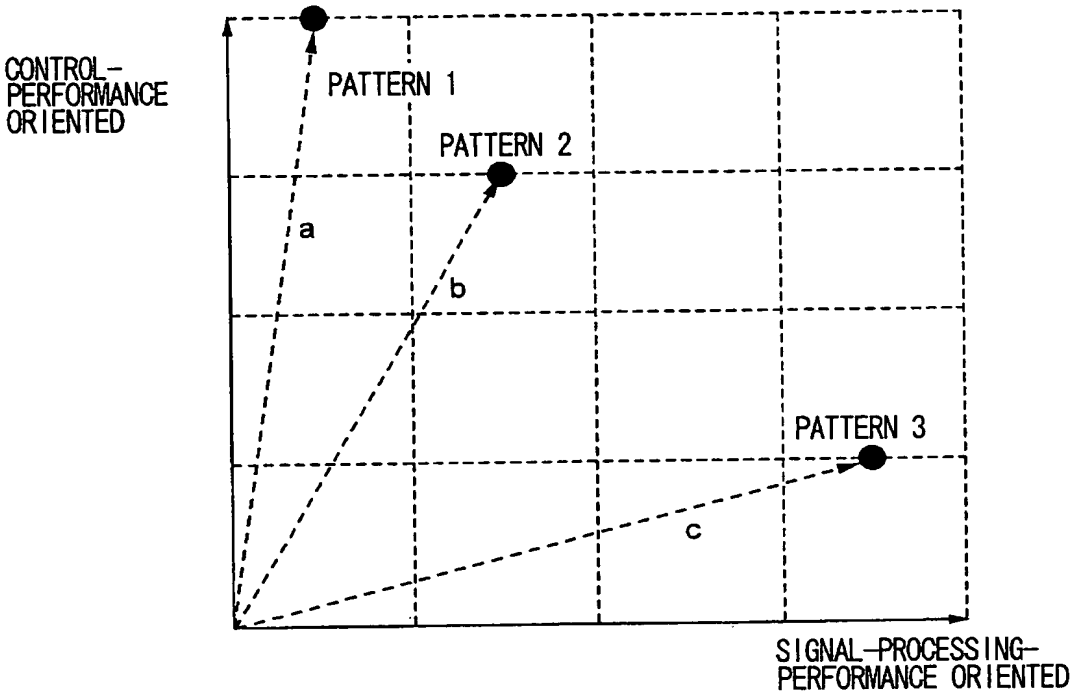


FIG . 6


CONTROL-
PERFORMANCE
ORIENTED
PATTERN 1
PATTERN 2
PATTERN 3
a
b
c
SIGNAL-PROCESSING-
PERFORMANCE ORIENTED

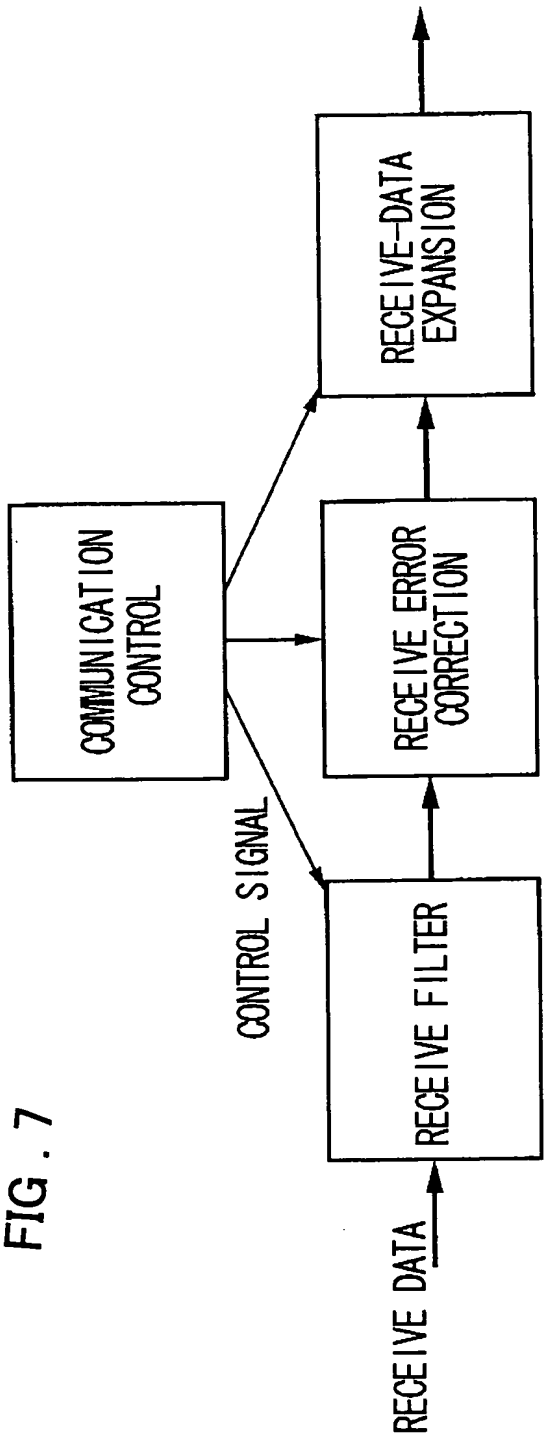

RECEIVE DATA
RECEIVE FILTER
RECEIVE ERROR CORRECTION
RECEIVE-DATA EXPANSION
COMMUNICATION CONTROL
CONTROL SIGNAL

FIG. 7

FIG. 8

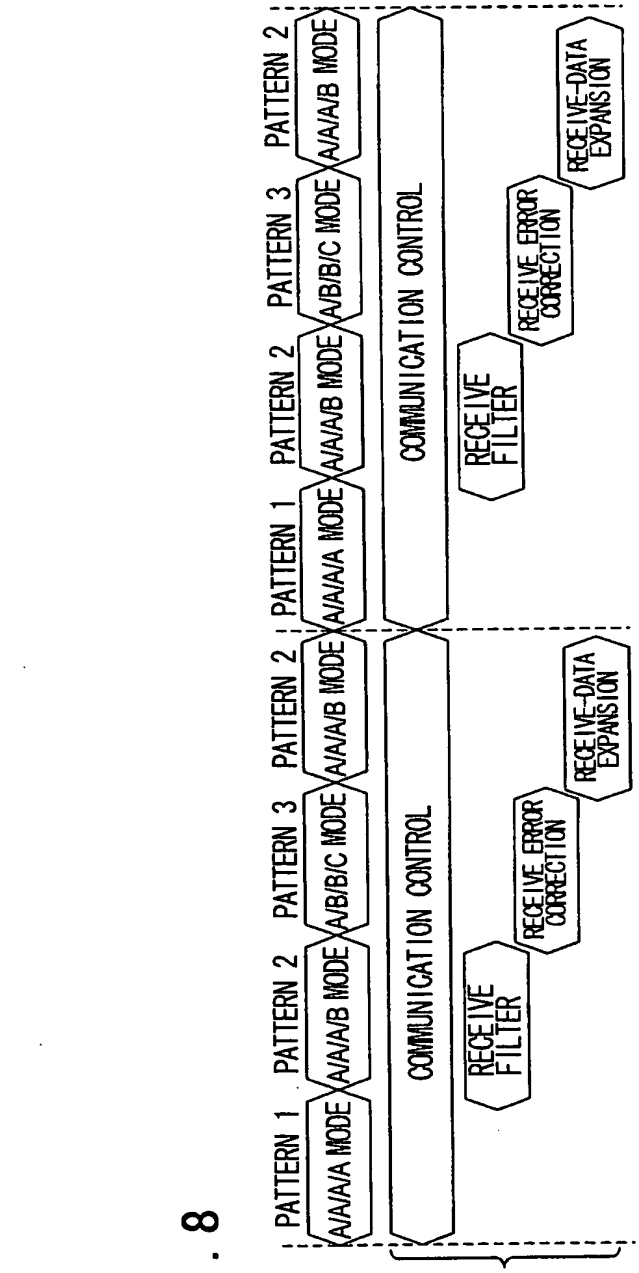

OPERATING PATTERN
PATTERN 1
A/A/A/A MODE
PATTERN 2
A/A/A/B MODE
PATTERN 3
A/B/B/C MODE
PATTERN 2
A/A/A/B MODE
PATTERN 1
A/A/A/A MODE
PATTERN 2
A/A/A/B MODE
PATTERN 3
A/B/B/C MODE
PATTERN 2
A/A/A/B MODE
APPLICATION
COMMUNICATION CONTROL
RECEIVE FILTER
RECEIVE ERROR CORRECTION
RECEIVE-DATA EXPANSION
COMMUNICATION CONTROL
RECEIVE FILTER
RECEIVE ERROR CORRECTION
RECEIVE-DATA EXPANSION

FIG . 9

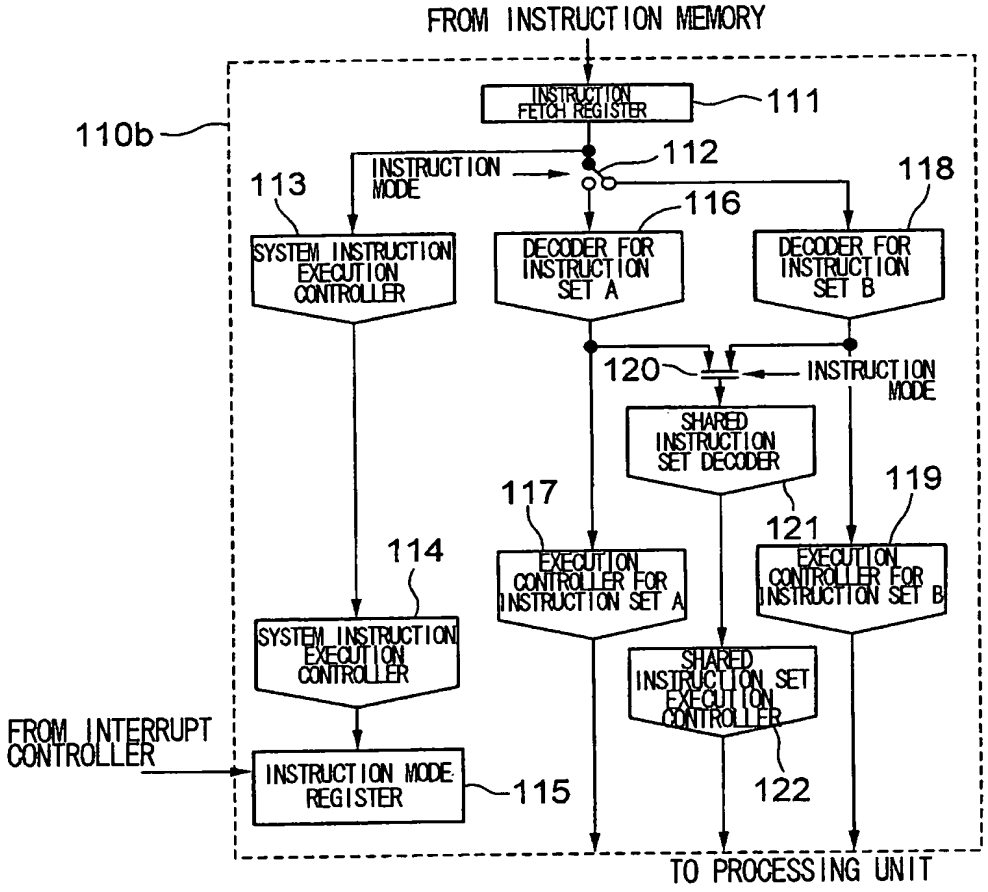

FROM INSTRUCTION MEMORY
110b
INSTRUCTION FETCH REGISTER
111
112
INSTRUCTION MODE
113
118
116
SYSTEM INSTRUCTION EXECUTION CONTROLLER
DECODER FOR INSTRUCTION SET A
DECODER FOR INSTRUCTION SET B
120
INSTRUCTION MODE
SHARED INSTRUCTION SET DECODER
117
119
121
114
EXECUTION CONTROLLER FOR INSTRUCTION SET A
EXECUTION CONTROLLER FOR INSTRUCTION SET B
SYSTEM INSTRUCTION EXECUTION CONTROLLER
SHARED INSTRUCTION SET EXECUTION CONTROLLER
FROM INTERRUPT CONTROLLER
INSTRUCTION MODE REGISTER
115
122
TO PROCESSING UNIT

FIG . 10

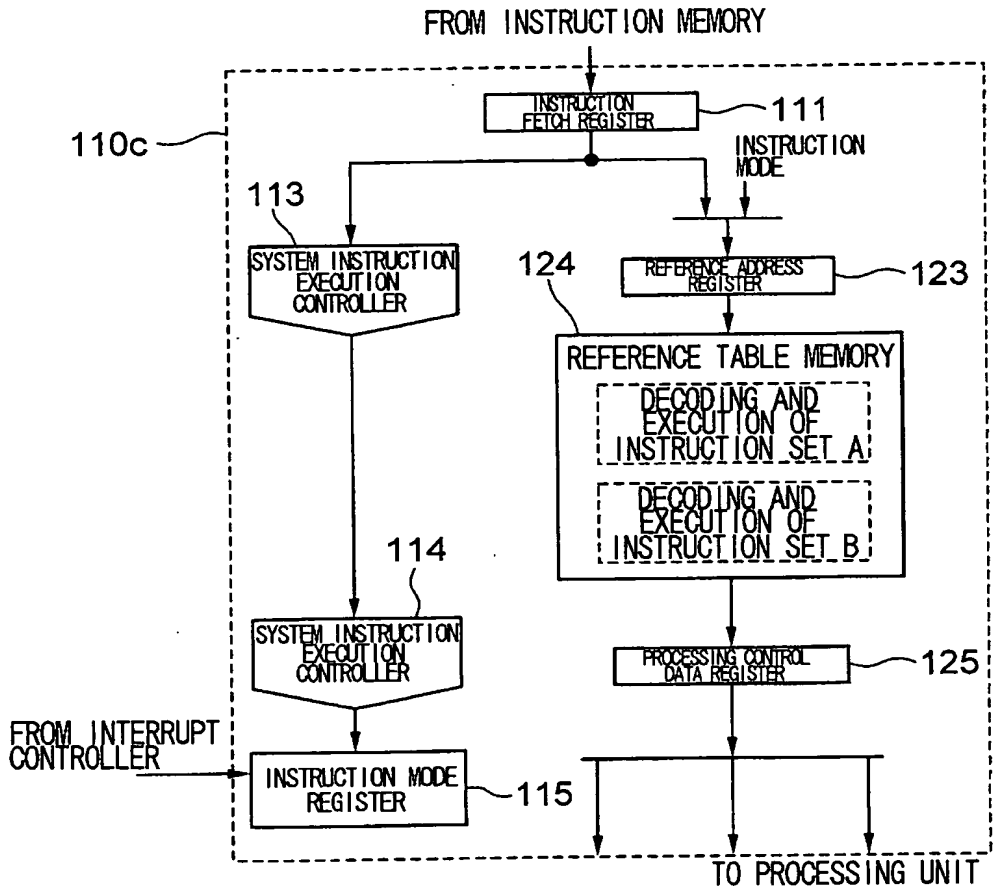

FROM INSTRUCTION MEMORY
INSTRUCTION FETCH REGISTER
111
110c
INSTRUCTION MODE
113
SYSTEM INSTRUCTION EXECUTION CONTROLLER
124
REFERENCE ADDRESS REGISTER
123
REFERENCE TABLE MEMORY
DECODING AND EXECUTION OF INSTRUCTION SET A
DECODING AND EXECUTION OF INSTRUCTION SET B
114
SYSTEM INSTRUCTION EXECUTION CONTROLLER
PROCESSING CONTROL DATA REGISTER
125
FROM INTERRUPT CONTROLLER
INSTRUCTION MODE REGISTER
115
TO PROCESSING UNIT

FIG. 11

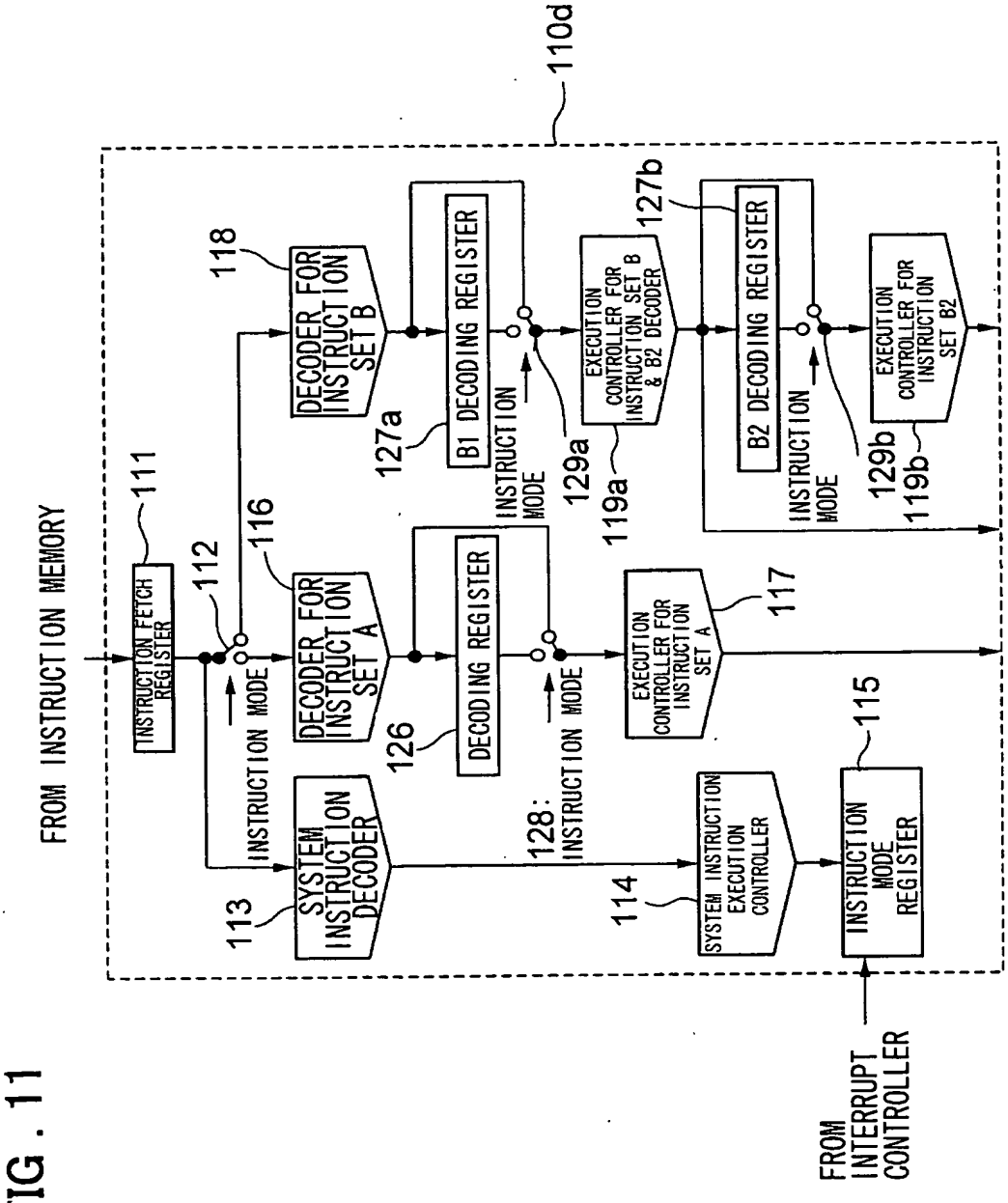

FROM INSTRUCTION MEMORY
110d
INSTRUCTION FETCH REGISTER
111
112
INSTRUCTION MODE
116
DECODER FOR INSTRUCTION SET A
126
DECODING REGISTER
INSTRUCTION MODE
EXECUTION CONTROLLER FOR INSTRUCTION SET A
117
118
DECODER FOR INSTRUCTION SET B
127a
B1 DECODING REGISTER
INSTRUCTION MODE
129a
EXECUTION CONTROLLER FOR INSTRUCTION SET B & B2 DECODER
119a
127b
B2 DECODING REGISTER
INSTRUCTION MODE
129b
119b
EXECUTION CONTROLLER FOR INSTRUCTION SET B2
TO PROCESSING UNIT
113
SYSTEM INSTRUCTION DECODER
128: INSTRUCTION MODE
114
SYSTEM INSTRUCTION EXECUTION CONTROLLER
115
INSTRUCTION MODE REGISTER
FROM INTERRUPT CONTROLLER

FIG . 12 PRIOR ART